UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,804	03/03/2004	Takashi Takamura	118577	4351

25944 7590 02/28/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
SEFER, AHMED N	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 02/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/790,804	TAKAMURA	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first partial buried region formed at a relatively deep position and the second partial buried region recited in claim 3 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2, 3, 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitations "a lower region ... has a relatively high impurity concentration" and "the first partial buried region formed at a relatively deep position and the second partial buried region" recited in claims 2 and 3 respectively are not clearly shown in the drawings. Furthermore, the limitation "the clear transistor includes the gate electrode ..." recited in claim 3 lacks sufficient antecedent basis -- if the output transistor and the clear transistor are sharing the same gate electrode, it should be stated so. For examining purposes, the said clear substrate region will be considered as the lower region and the accumulation region will be considered as a partial buried region.

While claim 3 recites "the first partial buried region ... and the second partial buried region," the limitation " ... the buried region functioning as a source region ..." recited in claim 5 does not specify which buried region.

The limitation "the first electrode ..." recited in claim 6 lacks sufficient antecedent basis.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-7 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7 of copending Application No. 10/790,868. Although the conflicting claims are not identical, they are not patentably distinct from each other because both the application and the copending application disclose similar solid-state imaging device.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Konishi et al. ("Konishi") US PG-Pub 4/0235261.

Konishi discloses in figs. 1-3 and 8 a solid-state imaging device, comprising: a pixel array having a plurality of pixels 10A arranged in a matrix; and a control unit 157 (par. 0075) that controls the pixel array; each of the pixels including: a photo diode 11 that generates carriers

depending on an intensity of incident light; an accumulation region 17 that accumulates the generated carriers; an insulated-gate 22 output transistor that outputs a signal according to a threshold voltage that changes depending on a number of the carriers accumulated in the accumulation region; and an insulated-gate clear transistor 13a that discharges the carriers accumulated in the accumulation region.

As for the recited operational limitations of the control unit and the clear transistor, claims directed to an apparatus must distinguish from the prior art in terms of structure rather than function, In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also In re Swinehart, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971; In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).

Regarding claim 2, as understood, Konishi discloses in fig. 3A a substrate region that is formed below the gate electrode of the clear transistor; and the substrate region comprising: an upper region 15 that is formed in a vicinity of the gate electrode of the clear transistor and that has a relatively low impurity concentration; and a lower region 18 that is formed below the upper region and that has a relatively high impurity concentration.

Regarding claim 3, as understood, Konishi discloses each of the pixels further comprising: a pixel-forming region 15 of a second conductivity type that is formed on a semiconductor substrate 14 of a first conductivity type and where at least one of the pixels is formed; a buried region of a first conductivity type that is formed in the pixel-forming region and that includes a first partial buried region 19 and a second partial buried region 17, the first partial buried region formed at a relatively deep position and having a relatively low impurity concentration, the second partial buried region formed at a relatively shallow position and

having a relatively high impurity concentration, the second partial buried region being the accumulation region; and a discharging region (par. 0079) of a first conductivity type that is formed in the pixel-forming region and into which carriers discharged from the accumulation region flow; an output transistor 12 that includes a gate electrode that is formed above the pixel-forming region on the accumulation region with an insulating film 21 therebetween; and the clear transistor includes the gate electrode 13a that is formed above the pixel-forming region between the buried region and the discharging region.

Regarding claim 4, as understood, Konishi discloses the photo diode including a junction region between the first partial buried region 19 and the pixel-forming region 15.

Regarding claim 5, as understood, Konishi discloses both the accumulation region 17 and the buried region 16 functioning as a source region of the clear transistor.

Regarding claim 6, as understood, Konishi discloses the first gate electrode 22 having a substantially annular shape; and the output transistor including a source region 23 that is formed inside the first gate electrode and a drain region 24 that is formed outside the first gate electrode.

Regarding claim 7, as understood, Konishi discloses the first conductivity type being a p-type; the second conductivity type being an n-type; and the carriers being holes.

8. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Dierickx US PG-Pub 2001/0011736.

Dierickx discloses in figs. 2 and 14 a solid-state imaging device, comprising: a pixel array having a plurality of pixels (par. 0035) arranged in a matrix; and a control unit (par. 0114) that controls the pixel array; each of the pixels including: a photo diode (par. 0063) that generates carriers depending on an intensity of incident light; an accumulation region 3 that

accumulates the generated carriers; an insulated-gate 7'/ 7 output transistor that outputs a signal according to a threshold voltage that changes depending on a number of the carriers accumulated in the accumulation region; and an insulated-gate clear transistor (par. 0073) that discharges the carriers accumulated in the accumulation region.

As for the recited operational limitations of the control unit and the clear transistor, claims directed to an apparatus must distinguish from the prior art in terms of structure rather than function, In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also In re Swinehart, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971; In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miida US PG-Pub 2002/016703 in view of Takizawa JP 2002-111960.

Miida discloses in figs. 1-8 a solid-state imaging device, comprising: a pixel array having a plurality of pixels (par. 0085) arranged in a matrix; and a control unit (par. 0095) that controls the pixel array; each of the pixels including: a photo diode 111 that generates carriers depending on an intensity of incident light; an accumulation region 25 that accumulates the generated carriers; an insulated-gate 112 output transistor that outputs a signal according to a threshold

voltage that changes depending on a number of the carriers accumulated in the accumulation region, but lacks anticipation of an insulated-gate clear transistor that discharges the carriers accumulated in the accumulation region.

Takizawa discloses in figs. 1-4 a solid-state imaging device, comprising: a pixel array having a plurality of pixels arranged in a matrix; and an insulated-gate 52 clear transistor that discharges the carriers accumulated in an accumulation region.

Since Miida and Takizawa are both from the same field of endeavor, solid-state imaging devices, Takizawa's teachings would have been recognized in the pertinent art of Miida. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate an insulated-gate clear transistor that discharges the carriers accumulated in an accumulation region with Miida's device, since that would improve charge transfer efficiency as taught by Takizawa.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
February 21, 2005

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800